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**UTILITY
PATENT APPLICATION
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(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

<i>Attorney Docket No.</i>	PD-99W231
<i>First Inventor or Application Identifier</i>	Reamon
<i>Title</i>	On-Chip Multilayer Metal Shielded Trans
<i>Express Mail Label No.</i>	EK444529438US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ * Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☒ Specification [Total Pages]
(preferred arrangement set forth below)
- Descriptive title of the Invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to Microfiche Appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets]
4. Oath or Declaration [Total Pages]
- a. ☐ Newly executed (original or copy)
- b. ☐ Copy from a prior application (37 C.F.R. § 1.6
(for continuation/divisional with Box 16 completed)
- i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting
inventor(s) named in the prior application
see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b)

5. ☐ Microfiche Computer Program (*Appendix*)
6. Nucleotide and/or Amino Acid Sequence Submission
(*if applicable, all necessary*)
- a. ☐ Computer Readable Copy
- b. ☐ Paper Copy (identical to computer copy)
- c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)
9. ☐ English Translation Document (if applicable)
10. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. ☐ * Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
(PTO/SB/09-12)
14. ☐ Certified Copy of Priority Document(s)
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Prior application information:

Examiner

Continuation-in-part (CIP)

of prior application No:

Group / Art Unit:

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Application Number	
Filing Date	
First Named Inventor	Reamon
Examiner Name	
Group / Art Unit	
Attorney Docket No.	PD-99W231

METHOD OF PAYMENT (check one)

- 1.
- ☒
- The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

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☐ Check ☐ Money Order ☐ Other**FEE CALCULATION****1. BASIC FILING FEE**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
101 760	201 380	Utility filing fee	690.00
106 310	206 155	Design filing fee	
107 480	207 240	Plant filing fee	
108 760	208 380	Reissue filing fee	
114 150	214 75	Provisional filing fee	

SUBTOTAL (1) (\$) **690.00****2. EXTRA CLAIM FEES**

Total Claims	Extra Claims	Fee from below	Fee Paid
14	-20**	78.00	78.00
4	-3**		
Independent Claims			
Multiple Dependent			

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description
103 18	203 9	Claims in excess of 20
102 78	202 39	Independent claims in excess of 3
104 260	204 130	Multiple dependent claim, if not paid
109 78	209 39	** Reissue independent claims over original patent
110 18	210 9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$) **78.00****FEE CALCULATION (continued)****3. ADDITIONAL FEES**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
105 130	205 65	Surcharge - late filing fee or oath	
127 50	227 25	Surcharge - late provisional filing fee or cover sheet.	
139 130	139 130	Non-English specification	
147 2,520	147 2,520	For filing a request for reexamination	
112 920*	112 920*	Requesting publication of SIR prior to Examiner action	
113 1,840*	113 1,840*	Requesting publication of SIR after Examiner action	
115 110	215 55	Extension for reply within first month	
116 380	216 190	Extension for reply within second month	
117 870	217 435	Extension for reply within third month	
118 1,360	218 680	Extension for reply within fourth month	
128 1,850	228 925	Extension for reply within fifth month	
119 300	219 150	Notice of Appeal	
120 300	220 150	Filing a brief in support of an appeal	
121 260	221 130	Request for oral hearing	
138 1,510	138 1,510	Petition to institute a public use proceeding	
140 110	240 55	Petition to revive - unavoidable	
141 1,210	241 605	Petition to revive - unintentional	
142 1,210	242 605	Utility issue fee (or reissue)	
143 430	243 215	Design issue fee	
144 580	244 290	Plant issue fee	
122 130	122 130	Petitions to the Commissioner	
123 50	123 50	Petitions related to provisional applications	
126 240	126 240	Submission of Information Disclosure Stmt	
581 40	581 40	Recording each patent assignment per property (times number of properties)	
146 760	246 380	Filing a submission after final rejection (37 CFR 1.129(a))	
149 760	249 380	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

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Signature

*Leonard A. Alkov*Date **11/02/00****Complete (if applicable)**Reg. Number **30,021**Deposit Account User ID **50-0616**

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ON-CHIP MULTILAYER METAL SHIELDED TRANSMISSION LINE

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Lloyd F. Linder
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Nick Elmi**

5 **ON-CHIP MULTILAYER METAL SHIELDED TRANSMISSION LINE**

10 **BACKGROUND OF THE INVENTION**

Field of Invention:

15 This invention relates to electrical circuit and systems. More specifically, the present invention relates to transmission lines.

Description of the Related Art:

20 In electrical circuit technology the advantages of a shielded signal path are well known. In transmission lines shielded conductors are widely used. The coaxial cable is an example of an improved transmission line having well known advantages stemming from its symmetry properties.

25 In microcircuits it has been long desired to achieve the advantages of shielded transmission lines, but planar fabrication techniques have not been acceptable to achieve this until now. The closest prior art, are the well-known on-chip stripline and the microstrip structures. These transmission line structures are not typically isolated well from surrounding electromagnetic fields. Improvements in isolation have been
30 achieved through physical separation from neighboring circuit elements and signal paths. However, this approach takes up valuable surface area on the chip.

There is a need for an isolated, shielded conductor used on-chip without consuming an inordinate amount of space. More specifically, there is a need for an isolated, shielded conductor used on-chip at radio frequencies (RF).

5

SUMMARY OF THE INVENTION

The need in the art is addressed by the on-chip multi-layer metal-shielded monolithic transmission line of the present invention. Generally, the inventive transmission line includes plural parallel planar thin film conductive layers and plural planar thin film nonconductive separator layers disposed such that each adjacent pair of the conductive layers is separated by a nonconductive layer to form a stack of alternating conductive and nonconductive layers.

15

In the illustrative embodiment, the invention is a planar structure with metal top and bottom planes and metal sidewalls produced by alternating thin film layers of conductors and insulators which are etched to successively build walls to a selected depth. Vias are filled with metal deposited so as to join adjacent metal layers. This four-sided metal "box" is fabricated with a metal conductor coaxially positioned to be shielded by the surrounding metal. Such structures may be constructed using standard planar technique in a side-by-side arrangement with or without common walls.

25

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is an elevational section view of a prior art stripline monolithic construction.

30

FIG. 2 is an elevational section view of a prior art microstrip monolithic construction.

FIG. 3 is an elevational section view of a 3 metal layer enablement of the present invention in a monolithic construction of a single signal conductor.

FIG. 4 is an elevational section view of a 5 metal layer enablement of the present invention in a monolithic construction of a single signal conductor.

FIG. 5 is an elevational section view of a 5 metal layer enablement of the present invention in a monolithic construction having multiple independent signal conductors.

FIG. 6 is a plan view of the present invention showing how elongated vias of the invention are staggered for signal isolation.

DESCRIPTION OF THE INVENTION

While the present invention is described herein with reference to illustrative embodiments for particular applications, it should be understood that the invention is not limited thereto. Those having ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope thereof and additional fields in which the present invention would be of significant utility.

Figs. 1 and 2 depict elevational section views of the prior art stripline and microstrip monolithic constructions respectively. Both of these constructions are well known in the planar fabrication and microcircuit technology. In Fig. 1, the stripline comprises a metal conductor etched on top of an insulator.

The microstrip construction shown in Fig. 2 comprises a pair of metal conductors in spaced apart positions with one of the conductors embedded within the insulation material. In both of these constructions, the only way to achieve field

isolation is to space adjacent conductors apart. However, this uses an undesirable amount of surface area on the substrate to achieve such isolation.

Referring to Fig. 3, an on-chip three layer metal-shielded monolithic
5 transmission line of the present invention comprises, in a simple embodiment, three parallel planar thin film, conductive layers 10 which are typically one micron thick condensates of Cu, Al, or Au placed by, for example, a physical vapor deposition process such as evaporation or sputtering. Each adjacent pair of the conductive layers
10 10 is separated by one of a plurality of planar thin film nonconductive separator layers 20, typically an oxide deposited or grown, to form a stack 30 of alternating conductive 10 and nonconductive 20 layers. An initial 12 and a final 14 ones of said conductive layers 10 form a top and a bottom conductive planes, the conductive planes establishing a mutually registered selected width 32 of the stack 30. A center one 16
15 16', 16" and 16''' separated laterally by a pair of nonconductive spacer layers 40, the two laterally terminal 16' and 16''' of the three conductive strips 16', 16" and 16''' being spaced at approximately the selected width 32.

Each of the nonconductive separator layers 20 provides a plurality of vias 22
20 between the two laterally terminal 16' and 16''' of the three conductive strips 16', 16" and 16''' and the conductive planes 12, 14. The vias 22 are cut into the separator layers 20, typically by dry etching processes that are well known, and are thereafter filled with conductive material 50, usually as part of the next metal layer deposition, for electrically interconnecting said conductive strips 16' and 16''' and the planes 12
25 and 14 so as to form a conductive side wall as part of a shield about the signal carrying centermost 16" of the three conductive strips 16', 16" and 16''' for electrical isolation thereof. The center strip 16" can be made approximately one micron in width and in height by process techniques well known to the planar fabrication engineer.

30

Referring to Fig. 4, the above-described configuration may be further extended to include additional layers such as the 5 metal layer embodiment shown. In this

further embodiment, the plurality of parallel planar thin film, conductive layers 10 are formed wherein each adjacent pair of the conductive layers is separated by one of the plurality of planar thin film nonconductive separator layers 20 to form the stack of alternating conductive and nonconductive said layers 30. The initial 12 and final 14
 5 ones of said conductive layers 10 form the top and bottom conductive planes as before, the conductive planes establishing the mutually registered selected width 32 of the stack. One of the conductive layers 16 between the top and the bottom conductive planes 12, 14, comprises three laterally spaced apart conductive strips 16', 16'', 16''' separated by a pair of nonconductive laterally spaced apart spacer layers 40, the two
 10 laterally terminal 16', 16'' of the three conductive strips being spaced approximately at the selected width 32 as in the previous embodiment.

Each of the other of the conductive layers 10 between the one of the conductive layers 16 and the top one of the conductive planes 14, and between the one
 15 of the conductive layers 16 and the bottom one of the conductive planes 12, comprises a pair of laterally spaced apart conductive strips separated by a nonconductive spacer layer 42 so that the pair of laterally spaced apart conductive strips are spaced approximately at the selected width, i.e., the stack width 32. Each of the nonconductive separator layers 20 provides a plurality of metal filled vias 22
 20 conductively joining the two outermost 16', 16''' of the three conductive strips of the one of the conductive layers 16, and the spaced apart conductive strips of the other of the conductive layers 10, and the conductive planes 12, 14 so as to form a conductive sidewall shield about the centermost 16'' of the three laterally spaced apart conductive strips.

25

Fig. 5 is a further embodiment of the construction techniques as described above, but for multiple independent shielded conductors when the constructions are side-by-side but share a common wall. As in the above discussion, the plurality of parallel planar thin film, conductive layers 10 are laid down, where, as defined above,
 30 each adjacent pair of the conductive layers 10 is separated by one of the plurality of planar thin film nonconductive separator layers 20 to form the stack of alternating conductive and nonconductive said layers. The initial and the final conductive layers

12, 14 form the top and the bottom conductive planes, the conductive planes establishing the mutually registered selected approximate width 32 of the stack 30.

One of the conductive layers 16 between the top 14 and the bottom 12
5 conductive planes comprises a plurality of N laterally spaced apart conductive strips 16', 16'', 16'''... 16^N, where N is an odd integer. Each laterally adjacent pair of the conductive strips, as for instance, 16' and 16'' is separated by the nonconductive spacer layer 40, and the two laterally terminal of the plurality of conductive strips, 16' and 16^N are spaced at the selected width 32 of the stack 30.

10 Each of the other of the conductive layers 10 between the one of the conductive layers 16 and the top one of the conductive planes 14, and between the one of the conductive layers 16 and the bottom one of the conductive planes 12, comprises a plurality of [(N-1)/2]+1 laterally spaced apart conductive strips, where each laterally
15 adjacent pair of the conductive strips is separated by a nonconductive spacer layer 42, the two laterally terminal of the plurality of conductive strips being spaced at the selected width 32 of the stack 30.

The nonconductive separator layers 20 provide the plurality of metal filled
20 vias 22, where the numeral 50 is meant to indicate the metal filling that occurs when the next conductive layer 10 is applied, as described above, positioned for electrically interconnecting the plurality of the conductive strips 10 so as to electrically isolate each of (N-1)/2 of the signal carrying conductive strips 16'', 16^{iv}, 16^v, etc. This enables the placement of any number of fully shielded signal carrying conductors in
25 side-by-side positions on the substrate. Because elongated vias 22 have a limited length, a limitation on the technology, as shown in Fig. 6, they are laid-out as a series of in-line constructions providing electrical interconnection between the metal strips, as previously described, but with spaces 24 where no interconnection metal 50 is able to be deposited.

30 As shown in the plain view of Fig. 6, because the vias 22 are generally only able to be fabricated with limited lengths "L", the spaces 24 between adjacent vias 22

of one shield side wall are staggered with respect to the spaces 24 between adjacent vias 22 of the adjacent next side wall so as to provide full isolation between adjacent center conductors 16' and 16" as, for instance, when the constructions defined above are positioned side-by-side on the substrate.

5

The method of making the on-chip multiple layer metal-shielded monolithic transmission line comprises the steps of forming the plurality of parallel planar thin film, conductive layers 10, by vapor deposition for instance, each in turn, separated by a plurality of planar thin film nonconductive separator layers 20, each also deposited or grown in turn, to form a stack 30 of alternating conductive and nonconductive said layers.

The process further comprises the step of extending, by simple metal deposition, the initial 12 and the final 14 ones of said conductive layers, as the top and the bottom conductive planes, to define the mutually registered selected width 32 of the stack 30.

Further, the inventive process includes the step of forming one layer 16, usually the center layer, of the conductive layers 10 between the initial (bottom) and the final (top) conductive planes 12, 14 into a plurality of N laterally spaced apart conductive strips 16', 16", etc., where N is an odd integer. This may be carried out by masking and etching steps as is well known in the art. Each of the adjacent pairs of the conductive strips are separated as well by the same technique so that each laterally adjacent pair of the conductive strips is interposed by a nonconductive spacer layer 40 and spacing the two laterally terminal of the plurality of conductive strips is such as to position then at the selected width 32 of the stack 30 by proper masking and registration steps as is well known in the art.

Likewise, the conductive layers 10 between the one of the conductive layers 16 and the top one 14 of the conductive planes, and between the one of the conductive layers and the bottom one 12 of the conductive planes are separated into a plurality of $[(N-1)/2]+1$ laterally spaced apart conductive strips as is shown in figures 4 and 5.

The vias 22 formed and positioned in nonconductive separator layers upon which metal layers are deposited are filled during the metal deposition process. This constructs a vertically continuous conductive wall to electrically interconnect the plurality of the conductive strips 10 so as to electrically isolate each of the (N-1)/2
5 signal carrying conductive strips which are positioned, preferentially at the geometric center of the stack, both horizontally and vertically.

The only process requirement is that the number of metal layers, be greater than 3. However, the fine line geometry of the metal used in BiCMOS or a fineline
10 multilayer CMOS process allows the thickness and minimum width of the metal conductor to be on the same order, thereby allowing the conductor to have the characteristics of an on-chip coaxial line. The novel structure is monolithic, exceeds typical isolation requirements, and uses significantly less surface area than microstrip or stripline structures in order to achieve the same isolation characteristics. A unique
15 feature of the implementation is the use of continuous vias so as to encase the center conductor. This feature maintains tight routing while meeting isolation requirements.

The invention provides an isolated on-chip coaxial conductor. Isolation is almost perfect in the present case. This is possible due to the use of multilayer metal
20 and nearly continuous interlayer metal via stacks along ground shield walls of the conductor. In the limit, conductor spacing can be minimized to a shared ground plane consisting of all layers of metal with nearly continuous stacked metal vias between these metal layers. This approach enables large matrix arrays to be implemented as monolithic structures so as to meet stringent isolation requirements while maintaining
25 a relatively small die size. Using multi-layer metal, internal layers can be used as ground planes to provide for the routing of multi-signal paths in a parallel fashion in the x- and y- directions. For example, a five layer metal process allows the placement of signal conductors on metal layers 2 and 4, with ground shielding on layers 1, 3, and 5. (Figure 3 extended from 3 layers to 5 layers).

30

In a preferred embodiment, five metal layers are placed and an isolated center conductor is provided. This allows a minimum impact from parasitics. From a

symmetry standpoint it allows the coaxial solution. For three or more layers the conductor is placed at the center of the stack of layers. Current fine geometry techniques enable dimensions of the conductor to approximate a coaxial line when shielded. An important feature is the stacked, stretched, multi-layer vias, which
5 enable nearly continuous closure of the center conductor, depending on the yield limits of a particular process technology for vias.

When adjacent conductors do not share a common ground shield, interlayer metal via stacks may be staggered. This approach eliminates any direct coupling
10 between two adjacent conductors. Increasing spacing between ground shields further isolates the signals.

Thus, the present invention has been described herein with reference to a particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications,
15 applications and embodiments within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications and embodiments within the scope of the present invention.

20

Accordingly,

WHAT IS CLAIMED IS:

CLAIMS

1. An on-chip multi-layer metal-shielded monolithic transmission line comprising:

plural parallel planar thin film, conductive layers and

5 plural planar thin film nonconductive separator layers disposed such that each adjacent pair of the conductive layers is separated by one of said plurality of planar thin film nonconductive layers to form a stack of alternating conductive and nonconductive layers.

2. The invention of Claim 1 wherein an initial and a final ones of said conductive layers form a top and a bottom conductive planes.

3. The invention of Claim 2 wherein the conductive planes are disposed to provide a mutually registered selected width of the stack.

4. The invention of Claim 3 wherein a center one of the conductive layers comprises three laterally spaced apart conductive strips.

5. The invention of Claim 4 wherein the conductive strips are separated by a pair of nonconductive spacer layers.

6. The invention of Claim 5 wherein two laterally spaced terminal strips of the three conductive strips are spaced at the selected width.

7. The invention of Claim 6 wherein the center conductive strips provides a signal carrying path.

8. The invention of Claim 7 wherein each of the nonconductive separator layers provide a plurality of vias between the two laterally spaced terminal strips of the three conductive strips and the conductive planes.

9. The invention of Claim 8 wherein the vias are filled with conductive material for electrically interconnecting said conductive strips and planes so as to form a conductive shield about the centermost of the three conductive strips for electrical isolation thereof.

10. An on-chip multilayer metal-shielded monolithic transmission line comprising:

a plurality of parallel planar thin film, conductive layers, each adjacent pair of the conductive layers separated by one of a plurality of planar thin film nonconductive separator layers to form a stack of alternating conductive and nonconductive said
5 layers;

an initial and a final ones of said conductive layers forming a top and a bottom conductive planes, the conductive planes establishing a mutually registered selected width of the stack;

10 one of the conductive layers between the top and the bottom conductive planes comprising three laterally spaced apart conductive strips separated by a pair of nonconductive spacer layers, the two laterally terminal of the three conductive strips being spaced at the selected width, the center one of the conductive strips providing a shielded signal carrying path;

15 each of the other of the conductive layers between the one of the conductive layers and the top one of the conductive planes, and between the one of the conductive layers and the bottom one of the conductive planes, comprising a pair of laterally spaced apart conductive strips separated by a nonconductive spacer layer so that the pair of laterally spaced apart conductive strips are spaced at the selected
20 width; and

each of the nonconductive separator layers providing a plurality of metal filled vias conductively joining the two outermost of the three conductive strips of the one of the conductive layers, and the spaced apart conductive strips of the other of the conductive layers, and the conductive planes, so as to form a conductive shield about
25 the centermost of the three laterally spaced apart conductive strips.

11. A plurality of on-chip multi-layer metal-shielded monolithic transmission lines comprising:

5 a plurality of parallel planar thin film, conductive layers, each adjacent pair of the conductive layers separated by one of a plurality of planar thin film nonconductive separator layers to form a stack of alternating conductive and nonconductive said layers;

an initial and a final ones of said conductive layers forming a top and a bottom conductive planes, the conductive planes establishing a mutually registered selected width of the stack;

10 one of the conductive layers between the top and the bottom conductive planes comprising a plurality of N laterally spaced apart conductive strips, where N is an odd integer, each laterally adjacent pair of the conductive strips separated by a nonconductive spacer layer forming $N-1/2$ signal carrying ones of the conductive strips, the two laterally terminal of the plurality of conductive strips being spaced at
15 the selected width;

each of the other of the conductive layers between the one of the conductive layers and the top one of the conductive planes, and between the one of the conductive layers and the bottom one of the conductive planes, comprising a plurality of $[(N-1)/2]+1$ laterally spaced apart conductive strips, each laterally adjacent pair of
20 the conductive strips separated by a nonconductive spacer layer, the two laterally terminal of the plurality of conductive strips being spaced at the selected width; and

the nonconductive separator layers providing a plurality of metal filled vias positioned for electrically interconnecting a plurality of the conductive strips so as to electrically isolate each of $(N-1)/2$ of the signal carrying conductive strips.

12. The transmission lines of Claim 11 wherein the vias of one of the transmission lines are staggered relative to the vias of an adjacent one of the transmission lines so as to preclude an electromagnetic line of sight path between the signal carrying conductive strips of the transmission lines.

13. A method of making an on-chip three layer metal-shielded monolithic transmission line comprising the steps of:

forming a plurality of parallel planar thin film, conductive layers, separated by a plurality of planar thin film nonconductive separator layers to form a stack of alternating conductive and nonconductive said layers;

extending an initial and a final ones of said conductive layers, as a top and a bottom conductive planes, to define a mutually registered selected width of the stack;

forming one of the conductive layers between the top and the bottom conductive planes into a plurality of N laterally spaced apart conductive strips, where N is an odd integer;

separating each laterally adjacent pair of the conductive strips by a nonconductive spacer layer and spacing the two laterally terminal of the plurality of conductive strips at the selected width;

separating each of the other of the conductive layers between the one of the conductive layers and the top one of the conductive planes, and between the one of the conductive layers and the bottom one of the conductive planes, into a plurality of $[(N-1)/2]+1$ laterally spaced apart conductive strips;

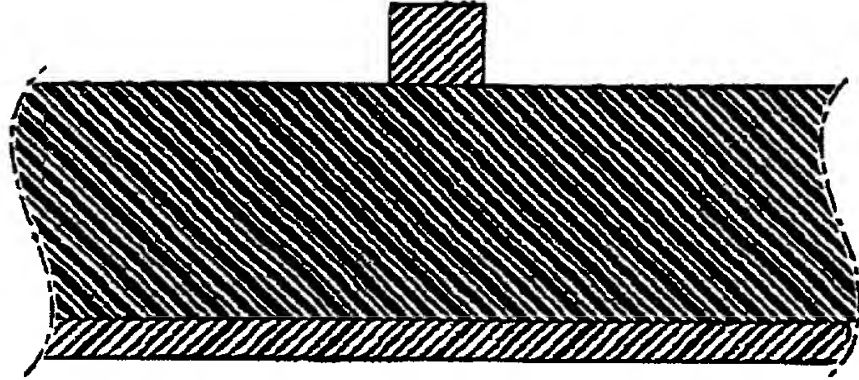
separating each laterally adjacent pair of the conductive strips by a nonconductive spacer layer, the two laterally terminal of the plurality of conductive strips being spaced at the selected width; and

filling a plurality of vias in the nonconductive separator layers with a conductor material to electrically interconnect a plurality of the conductive strips so as to electrically isolate each of $(N-1)/2$ signal carrying ones of the conductive strips.

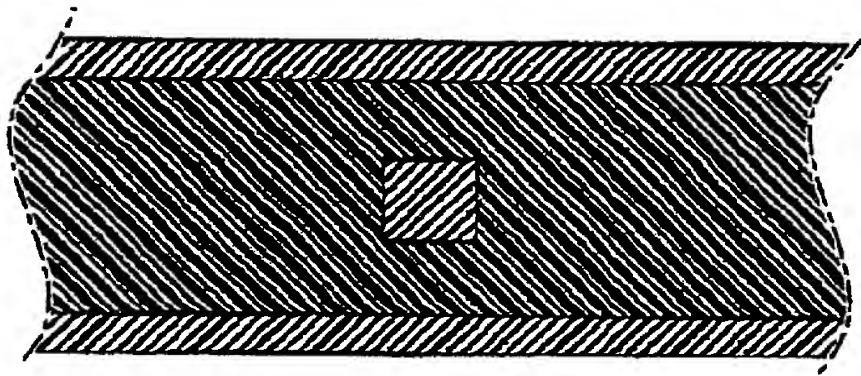
14. The method of Claim 13 further comprising the step of staggering the position of the vias of one of the transmission lines relative to the vias of an adjacent one of the transmission lines so as to preclude an electromagnetic line of sight path between the signal carrying conductive strips of the transmission lines.

ABSTRACT OF THE DISCLOSURE

Multi-layer metal-shielded monolithic transmission lines are formed in side-by-side arrangement by depositing parallel planar thin film, conductive layers, separated by nonconductive separator layers to form a stack of alternating conductive and nonconductive layers. The conductive layers form a top and a bottom conductive plane and establish a mutually registered selected width of the stack. A center
5 conductive layer has laterally spaced apart conductive strips separated by nonconductive spacer layers. The two laterally terminal of the conductive strips are spaced at the selected width. Each of the nonconductive separator layers provides a plurality of elongated vias between the two lateral terminals of the three conductive
10 strips and the conductive planes. The vias are filled as each next metal deposition is applied for electrically interconnecting the conductive strips and planes so as to form a monolithic conductive shield about the centermost signal carrying conductor of the three conductive strips, providing electrical isolation in a coaxial arrangement.



Prior Art
Fig. 1



Prior Art
Fig. 2

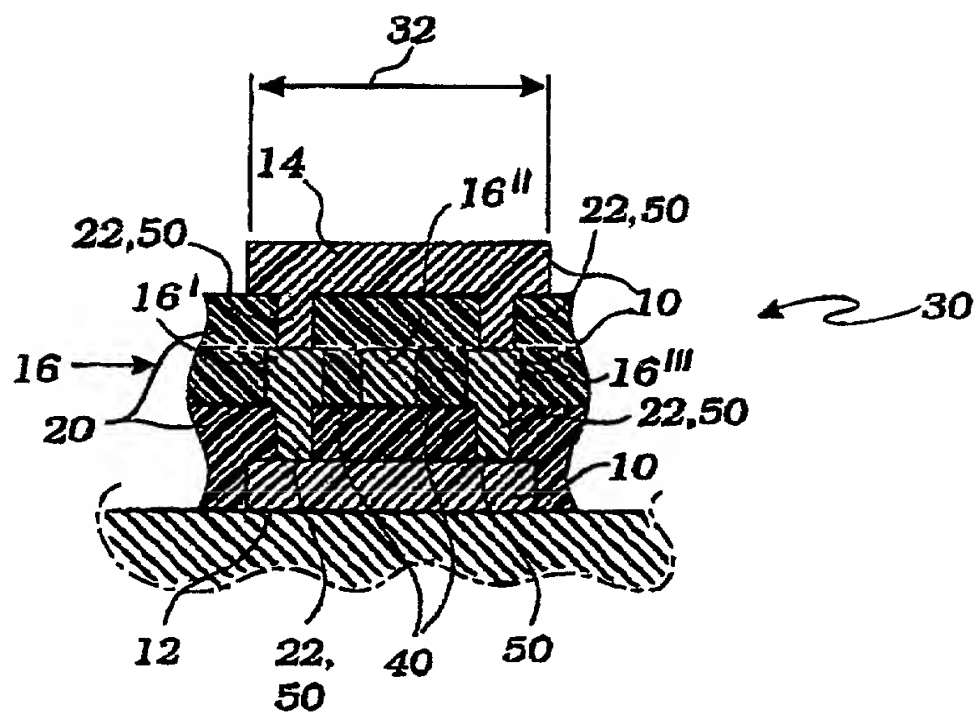


Fig. 3

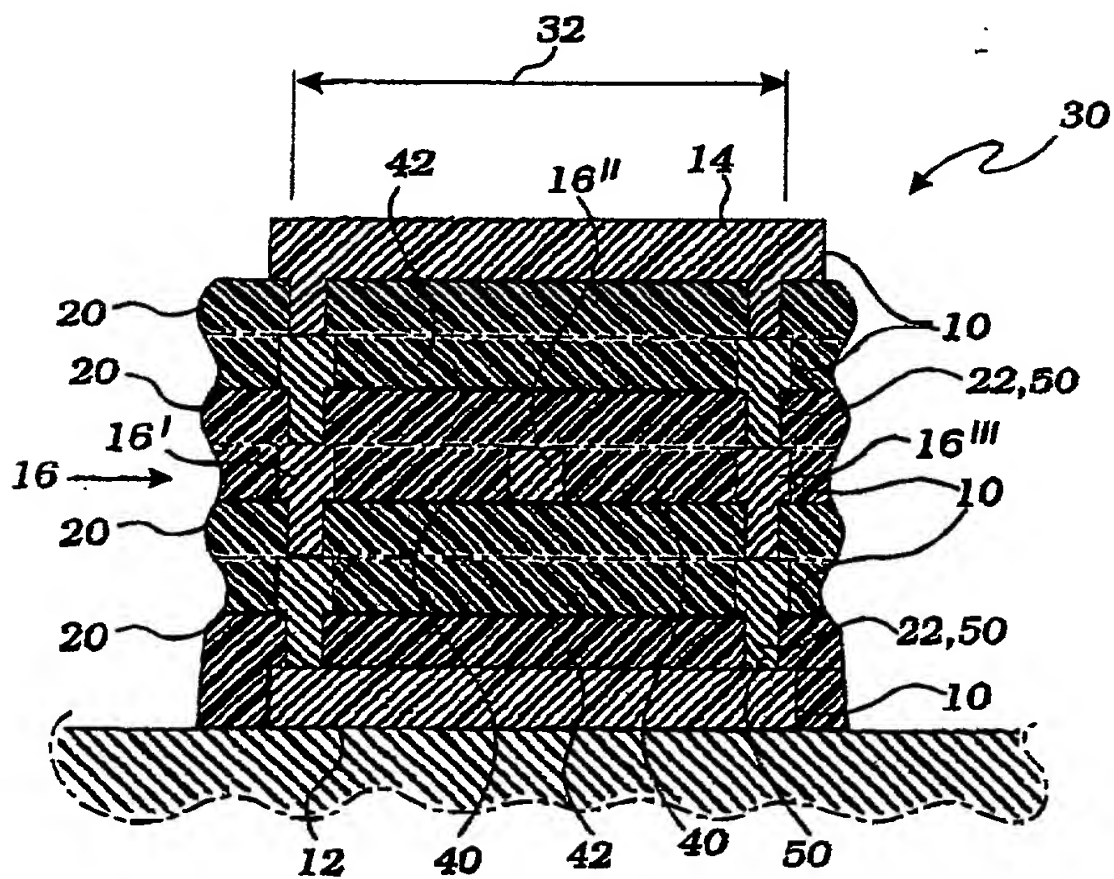


Fig. 4

